UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,380	03/17/2004	Anthony Cake	455610-2490.1	3812

20999 7590 01/12/2005

FROMMER LAWRENCE & HAUG
745 FIFTH AVENUE- 10TH FL.
NEW YORK, NY 10151

EXAMINER	
BLACKMAN, ANTHONY J	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/802,380	CAKE ET AL.	
	Examiner	Art Unit	
	ANTHONY J BLACKMAN	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-44* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/16/04*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *1/4/05*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 12/16/04 is being considered by the examiner.

Claim Objections

2. Claim 42 is objected to because of the following informalities: line 2 should read, update of said first processing element (the word [of] was left out due to a typing error). Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 22 and 25-40, and 43-44 are rejected under 35 U.S.C. 102(e) as being anticipated by ZINK et al, US Patent No.6,738,964.

5. As per claim 22, examiner interprets ZINK et al to disclose the following features and limitations as recited; A method for modifying a processing sequence (column 7, lines 50-57) by editing the configuration of a processing web (column 6, lines 12-24), comprising the steps of:

determining a current state of said processing web (the component creator determines the state/what properties will be included in a component, whether the properties can be modified and when the properties are accessible– column 7, lines 50-57and figure 23 illustrates how a script may query the environment to achieve a particular result is equivalent to the feature as claimed – see column 24, lines 36-67); and

editing at least one processing element of said processing web (the component assembly tool performs editing and the components and blocks are equivalent to processors– column 6, lines 12-24),

whereby said processing sequence is modified in accordance with the editing of said at least one processing element (column 6, lines 12-24).

6. As per claim 25, ZINK et al meet limitations and features of claim 22, including, wherein said editing of said at least one processing element includes changing a connection of at least one pin of said at least on processing element (column 20, lines 19-29).

7. As per claim 26, ZINK et al meet limitations and features of claim 22, including, wherein said editing of said at least one processing element includes adding another processing element to said processing web (is equivalent to the component creator adding at least event inputs and outputs, see - column 20, lines 19-29).

8. As per claim 27, ZINK et al meet limitations and features of claim 26, including, wherein said another processing element is added to said processing web by dragging a representation of said processing element onto a display representative of said processing web (column 6, lines 12-24), and connecting inputs and outputs of said another processing element to the inputs and outputs of other existing processing elements (column 20, lines 19-29).

9. As per claim 28, ZINK et al meet limitations and features of claim 22, including, wherein said editing of said at least one processing element includes modifying the definition thereof (the component assembly tool 507 comprises a drag and drop means to facilitate "component assembly"/editing/modifying and further the component creator, see column 7, lines 50-57, also determines what properties will be included, whether they can be modified, and when they are accessible provides an equivalent to modifying the definition).

10. As per claim 29, ZINK et al meet limitations and features of claim 28, including, wherein modifying the definition of said at least one processing element includes modifying one or more operating parameters thereof (the component assembly tool 507 comprises a drag and drop means to facilitate "component assembly"/editing/modifying and further the component creator , see column 7, lines 50-57, also determines what properties will be included, whether they can be modified, and when they are accessible provides an equivalent to modifying at least one of the parameters).

11. As per claim 30, ZINK et al meet limitations and features of claim 22, including, , further comprising the step of adding a viewing element to said graphical representation

of said processing web to view a live, real time output at the location of said viewing element (see the Data viewer applets - column 6, lines 42-53)

12. As per claim 31. A method for modifying a processing sequence (column 7, lines 50-57) by editing the graphical representation of a processing web as displayed on a processing web editor (column 6, lines 12-24), comprising the steps of :

determining a current state of said processing web (the component creator determines the state - 7, lines 50-57 57and figure 23 illustrates how a script may query the environment to achieve a particular result is equivalent to the feature as claimed – see column 24, lines 36-67);

generating a graphical representation of said processing web (column 6, lines 12-24) by: determining a first processing element of said processing web (figure 9, element 1001 is the first of many connective blocks equivalent to processing elements, see column 8, line 38-column 9);

placing said first processing element (figure 9, element 1001 is equivalent to a processing element) in a particular location based at least

in part upon its location in said processing web and various inputs to and outputs from said first processing element/figure 9, element 1001 (placement is inherent as with figure 9, element 1001 and 1002 and so on –column 8, line 38-column 9, line 9);

determining a second processing element of said processing web (figure 9, element 1002 pursuant to element 1001 see column 8, line 38-column 9, line 9);

placing said second processing element in a particular location based at

least in part upon its location in said processing web (placement is inherent as with figure 9, element 1001 and 1002 and so on –column 8, line 38-column 9, line 9), various inputs to and outputs from said second processing element (column 8, line 38-column 9, line 9 , including figure 8a that shows "various inputs and outputs"), and a relationship between said second processing element and said first processing element (figure 9, elements 1001 and 1002 represent separate processors (claimed) and connective blocks see column 8, lines 38-column 9, line 9); and

connecting at least one pin of said first processing element to one pin of said second processing element (this feature is inherent between elements 1001 and 1002 and supported by figures 8a-8d), and

editing at least one processing element of said processing web (the slide control 1008 modifies the sine wave generator 1001 see column 8, lines 49-55);

whereby said processing sequence is modified in accordance with the editing of said at least one processing element (the action of the slide control 1008 modifies the sine wave generator 1001 and further modification is performed by element 1009 on element 1002- see column 8, lines 49-62).

13. As per claim 32. A graphical representation of a processing web of an instrument (figure 9 and column 8, line 38-column 9, line 9) , comprising:

a first processing element of said processing web (figure 9, element 1001 is the first of many connective blocks equivalent to processing elements, see column 8, line 38-column 9); said first processing element being placed in a particular location based at

least in part upon its location in said processing web (placement is inherent as with figure 9, element 1001 and 1002 and so on –column 8, line 38-column 9, line 9) and various inputs to and outputs from said first processing element (placement is inherent as with figure 9, element 1001 and 1002 and so on –column 8, line 38-column 9, line 9), a second processing element of said processing web (figure 9, element 1002, pursuant to element 1001 is at least one set of connective blocks equivalent to processing elements, see column 8, line 38-column 9), said second processing element in a particular location based at least in part upon its location in said processing web(placement is inherent as with figure 9, element 1001 and 1002 and so on –column 8, line 38-column 9, line 9) , various inputs to and outputs from said second processing element (figure 9, elements 1001 and 1002, column 8, line 38-column 9, line 9), and a relationship between said second processing element and said first processing element (column 8, lines 38-62); and

a connection for connecting at least one pin of said first processing element to one pin of said second processing element (this feature is inherent between elements 1001 and 1002 and supported by figures 8a-8d and 9).

14. As per claim 33, ZINK et al meet limitations and features of claim 32, including, wherein said connection connects an output pin of said first element to an input pin of said second element (figure 9, first and second elements, 1001 and 1002 are connected by element 1004. See column 20, lines 19-29 for support of the component author/creator editing use of connecting pin means) .

15. As per claim 34, ZINK et al meet limitations and features of claim 33, including, wherein said connection generates a line in said graphical representation between said output pin of said first element to said output pin of said second element (column n8, lines 25-37).

16. As per claim 35, ZINK et al meet limitations and features of claim 33, including, wherein said line is drawn including one of a plurality of designations based upon a type of data being carried thereon (column 8, lines 25-37).

17. As per claim 36, ZINK et al meet limitations and features of claim 35, including, wherein said plurality of designations are colors (column 7, lines 19-29 and column 8, lines 25-37).

18. As per claim 37, ZINK et al meet limitations and features of claim 32, including, wherein said at least one pin of said first processing element and said at least one pin of said second processing element are coded based upon a type of data to output thereon, or received thereby, respectively (the wires are equivalent to pins and "any pin may be located at any position along the periphery of the block" - column 7, lines 19-23 and lines 24-28 and column 8, lines 25-37).

19. As per claim 38, ZINK et al meet limitations and features of claim 37, including, wherein said coding is by color (column 7, lines 19-28 and column 8, lines 25-37).

20. As per claim 39, ZINK et al meet limitations and features of claim 37, including, wherein said coding is by symbol (it is inherent that the data wires , 1004 and 1005 are equivalent to the symbols as claimed - column 8, lines 25-37).

21. As per claim 40, ZINK et al meet limitations and features of claim 23, including, wherein said coding is by graphical designation (it is inherent that the data wires , 1004 and 1005 are equivalent to the symbols as claimed - column 8, lines 25-37).

22 As per claim 43, ZINK et al meet features and limitations of claim 41, wherein said update of said first and second processors is controlled by an update processing element (column 16, line 65-column 17, line 10).

23. As per claim 44, ZINK et al meet limitations and features of claim 32, including, wherein a viewing object may be placed at any location on the graphical representation to see a current, live output at that location (the data viewer applet 508 at column 6, lines 42-53).

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over ZINK et al, US Patent No. 6,738,964 in view of WILSON et al, US Patent No. 5,400,246.

26. As per claim 23, ZINK et al meet limitations of claim 22, however, does not expressly teach further comprising the step of said first processing element indicating

a time during which said first processing element is to consume additional input data/updating the values. WILSON at least suggests further comprising the step of said first processing element indicating a time during which said first processing element is to consume additional input data/updating the values (column 30, lines 3-22 and 38-51 indicate current status means). It would have been obvious to one skilled in the art at the time of the invention to utilize the following features and limitations of ZINK et al; "In review, it can now be seen that the present invention provides a peripheral data acquisition, monitor, and adaptive control system which allows the user to easily create, modify, and test complex control system configurations on a personal computer. The program can be configured to orient the user with respect to the physical location and function of the equipment being controlled by the system column 35, lines 9-16" of WILSON et al to modify the hardware and software graphical solutions development system of ZINK et al because WILSON et al's "...adaptive control system which allows the user to easily create, modify, and test complex control system configurations on a personal computer (column 35, lines 9-16) providing greater user operability and control in monitoring the development system of ZINK et al. Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify ZINK et al with WILSON et al.

27. As per claim 24, ZINK et al meet limitations and features of claim 23, however, does not expressly teach wherein said update is controlled by an update processing element . WILSON et al at least suggest wherein said update is controlled by an update processing element (column 30, lines 3-22 and 38-51 indicate current

status means discuss the means of an update processing element that bears similar results to the recited claim language). It would have been obvious to one skilled in the art at the time of the invention to utilize the following features and limitations of ZINK et al; "In review, it can now be seen that the present invention provides a peripheral data acquisition, monitor, and adaptive control system which allows the user to easily create, modify, and test complex control system configurations on a personal computer. The program can be configured to orient the user with respect to the physical location and function of the equipment being controlled by the system column 35, lines 9-16" of WILSON et al to modify the hardware and software graphical solutions development system of ZINK et al because WILSON et al's "...adaptive control system which allows the user to easily create, modify, and test complex control system configurations on a personal computer (column 35, lines 9-16) providing greater user operability and control in monitoring the development system of ZINK et al. Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify ZINK et al with WILSON et al.

28. Claims 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over ZINK et al, US Patent No. 6,738,964 in view of HORST et al, US Patent No. 5,384,906.

29. As per claim 41, ZINK et al meet limitations of claim 32, however, does not teach wherein the first processing element is updated at a faster rate and said second processing element is updated at a slower rate. HORST teaches wherein the first processing element is updated at a faster rate and said second processing element is updated at a slower rate (updating is equivalent to configuring - column 3, lines 21-39

"...allows two or more processors to be configured in a fault detecting
or fault tolerant arrangement without the need for a fault tolerant clock
circuit. The processors are free to execute the same algorithm at different
speeds, whether due to differences in clock rates or the occurrence of "extra"
clock cycles."

It would have been obvious to one skilled in the art that updating/configuring two processors that are different rates for the purpose of synchronizing said processors to modify the graphical solutions development system for software or software/hardware hybrids with intelligent development components appropriate for real-time processors plus development framework rules to insure development component object optimization within the resulting application program (column 1, lines 42-50) of ZINK et al because both inventions are related to multiple processor operations, particularly, the addition of HORST provides "...loosely synchronizing a plurality of processors (column 3, lines 23-25)", i.e., as shown above, for processors with different updating/configuring rates. Therefore, it would have been obvious to use HORST to modify ZINK et al.

30. As per claim 42, ZINK et al as modified meet limitations of claim 41, however, ZINK et al does not teach the following feature and limitation as recited, wherein said update [of] said first said first processing element and update of said second processing element are synchronized (column 3, lines 21-39).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANTHONY J BLACKMAN whose telephone number is 703-305-0833. The examiner can normally be reached on FLEX SCHEDULE Monday through Friday between the hours of 8am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MATTHEW BELLA can be reached on 703-308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANTHONY J BLACKMAN
Examiner
Art Unit 2676

***

MATTHEW LUU
PRIMARY EXAMINER